Exam Seat No:_____ **Enrollment No:_____**

C.U.SHAH UNIVERSITY

WADHWAN CITY

University (Winter) Examination -2013

Course Name :M.Tech(EC)Sem-I **Subject Name: -ASIC *DESIGN*** **Duration :- 2:30 Hours**

Date : 13/1/2014 **Marks : 70**

Instructions:-

(1) Attempt all Questions of both sections in same answer book / Supplementary.

(2) Use of Programmable calculator & any other electronic instrument is prohibited.

(3) Instructions written on main answer Book are strictly to be obeyed.

(4) Draw neat diagrams & figures (If necessary) at right places.

(5) Assume suitable & Perfect data if needed.

SECTION-I

Q:-1	i	Define terms: Basic identifiers	1
	ii	What is signal driver?	1
	iii	What is ASIC?	1
	iv	Explain following terms with reference to VHDL. (1) Generate statement (2) Wait Statement	2
	v	Draw ASIC design flow.	2
Q:-2	A	Give the Generic Architecture for following devices PLA, PAL.	4
	B	Write VHDL code for Binary to Gray code conversion.	5
	C	Explain process statement. Explain the importance of sensitivity list. Quote suitable example.	5
		OR	
Q:-2	A	Differentiate between signal & variable.	4
	B	Write VHDL code for 1 to 8 lines multiplexer.	5
	C	Explain the importance of Regularity, Modularity and Locality terms in ASIC design. with help of suitable example.	5
Q:-3	A	Describe various data types used in VHDL.	7
	B	Explain transport delay model & inertial delay model. Also give comparison between them.	7
		OR	
Q:-3	A	Explain various predefined operators in VHDL with their precedence.	7
	B	Write How to design & integrate modulo-10 down counter using VHDL.	7

SECTION-II

Q:-4	i	Define Data flow modelling.	1
	ii	What is PLD?	1
	iii	What is the use of attribute in VHDL?	1

	iv	Define the following terms (1) Alias (2) Package	2
	v	Differentiate between exit & next statement.	2
Q:-5	A	Do as directed. (1) Briefly describe necessity of configuration. (2) Elaborate package declaration.	4
	B	Compare concurrent signal assignment & sequential signal assignment with example.	5
	C	Write the VHDL code for the 4 to 16 lines decoder using behavioural style of modelling.	5

OR

Q:-5	A	What is test bench? Write typical test bench format.	4
	B	Briefly describe implicit & explicit visibility in VHDL.	5
	C	Using structural method. write a VHDL code for (4-bit) binary parallel adder. Take 1-bit full adder as a component.	5
Q:-6	A	Discuss Moore & Mealy State Machine with example.	7
	B	Draw & explain FPGA Architecture.	7

OR

Q:-6	A	List down the advantages & disadvantages of finite state machine.	7
	B	Explain assertion statement. Explain its use fulness in writing test bench.	7

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